The following provides a high-level overview of the RDB350 Access point (AP)/Remote module (RM). The RDB350 Transceiver board consists of base band digital section and RF analog section:

Base band section: The brain of the system is the base band SoC (System-on-a-Chip) processors running at 180 MHz. This device has a Fast Ethernet Controller, which allows a 10/100 Base-T implementation. The interface is implemented using magnetics, 10/100 Fast PHY device, and Ethernet MAC implemented in the SoC. The interface between the Fast PHY and the SoC is an MII interface.

The Ethernet interface in the design has four main purposes:

Power supply to the unit (POE+)

Data port

Management port

Unit synchronization

The power to the unit is supplied over a standard Ethernet category 5 cable. The cable length is up to 100m. The power supply scheme is standard power over Ethernet (POE+) that can drive more than 30 watt to the unit.

Free running 25MHz (+/-50PPM) oscillator is used for driving the Fast Ethernet PHY reference clock input for proper operation. The Ethernet interface supports speed rates of up to 100Mbit/sec full duplex.

The Ethernet data port is also used for in-band management.

Unit synchronization is achieved by translating the GPS 1PPS pulse required for synchronization.

The SoC also interfaces with the Flash and SDRAM, on the data and address buses for storing Data Queues, SW program and data.

The Ethernet data packets are passed to the SDRAM using SDRAM controller inside SoC running at 90 MHz. The SoC complies with 802.16e WiMAX standard protocols for over the air communications with Subscriber Modules or CPEs. The SoC classifies the incoming packets into an 802.16e compliant bitstream and tunnels through Packet Data Units (PDU's) from various application protocols like Ethernet (IEEE 802.3) between PMP320 AP and CPEs. Additionally, 802.16e Medium Access Controller (MAC) Layer and Physical (PHY) Layer features are supported by SoC.

RS232 UART interface is used in debug mode to enable factory and lab a simple channel of communication to the AP.

The power supply architecture is designed to drive all operating voltage level required by the various system components. It is constructed of switched and linear regulators to fit the design requirement for efficiency as well as for noise immunity.

A temperature sensor is used to measure the unit ambient temperature read by SoC. This is an SPI-interface component that is connected to one of the SoC timed SPI interfaces.

The debug connectors are available for general purpose debugging and SoC processors debugging.

LEDs are implemented to provide user with unit status. The LEDs are AP Synchronization indication, GPS signal availability visual indication, Power visual indication, link status visual indication and, ETH visual indication TX/RX.

Clock Distribution:

The clock distribution circuitry is responsible for distributing an accurate and stable clock to the components of the design. The clock accuracy and stability is up to +/-2PPM (over temperature, other instability factors are system compensated).

The circuitry is constructed of TCXO, Clock driver, External clock input connector (debug use), External clock output connector (debug use) and LDO regulator.

The system requirement of +/-2PPM defines the use of an accurate oscillator like a 40 MHz TCXO.

The clock driver distributes the clock source to two receiver and two transmitter RF sections, SoC and External clock output connector.

RF Analog Section: The heart of the system is RF section which supplies the network with DownLink/UpLink wireless data to/from subscriber modules (SMs) or CPEs. RF analog section up converts the outgoing 802.16e WiMAX bitstream baseband data (DownLink) from PHY layer into analog domain and transmits it to the SMs or CPEs. Also, the received analog signal from SMs is down converted to Baseband digital signal (UpLink) and passed to PHY layer.

The RFIC AD9355 transceiver is used which meets IEEE 802.16e WiMAX requirements. The component supports the frequency band of 4.4GHz – 4.99GHz.

The RFIC AD9355 is a RF MISO (Multiple Input/Single Output) transceiver with integrated ADCs and DACs for a digital base band interface. The signals in the RF side are 4.x GHz differential signals.

In order to increase system performance advanced antenna techniques are introduced. The system supports 2x2 MIMO (two transmit and two receive) configuration.

Two RF analog sections are required and implemented for two independent transmit and receive chains.

Transmitter:

The RF TX path consists of the RFIC, PA, LPF, and TX&RX switch.

The Base Band digital TX signal from PHY layer is interpolated, filtered and converted to an analog signal by RFIC. The RFIC IQ modulates the signal and control the signals gain. Finally, the RFIC up converts the frequency to 4.x GHz band and delivers the signal terminated differentially (50 Ω).

The BALUN translate the differential signal to a single ended with 50 ohm termination. The BPF filters out of band spurious emitted from the RFIC.

The PA amplifies the signals power and Low Pass Filters are used to eliminate out of band spurs and harmonics.

The TX&RX switch directs the TX signal to the antenna

The MCX connector is the connection to the antenna.

The SoC supports closed loop and open Loop transmit power control according to IEEE 802.16e standard. This power is expressed in 0.25 dB steps with 58dB range, from +27dBm to -31dBm. Due to the gain variation over temperature, the TX chain may require a back off.

Receiver:

The RF RX path mainly consists of the RFIC, LNA, BPF and TX&RX switch.

The MCX connector is the connection to the antenna. The Analog signal from the antenna is received towards the TX&RX switch. The TX&RX switch direct the signal to the RX path. The BPF limits the spectral power and filters out of band spurs. The LNA amplifies the signal. The digital variable attenuator used to calibrate the receive chains. The BALUN translates the single ended signal to differential (50 Ω). The RFIC down converts the signals frequency from 4.x GHz band. The RFIC control the signals gain and IQ demodulate the signal. The RFIC converts the signal from analog to digital, filters and decimate the signal.

The RFIC drive the base band signal towards the SoC where the base band signal is demodulated and channel decoded based on 802.16e WiMAX standard PHY functions